Application No.: 09/990,397
Docket No.: JCLA7289

REMARKS

Present Status of Application

The Office Action mailed December 19, rejected claims 1, 2 and 4-13 under 35 U.S.C. § 103(a) over Park (US Patent 6,100,559) in view of Bui (US Patent 6,163,049). The Office Action objected to drawings and the specification for informalities. The specification and drawings have been amended. This amendment is promptly filed to place the above-captioned case in condition for allowance. No new matter has been added to the application by the amendments made to the claims, specification or otherwise in the application. After considering the following remarks, a notice of allowance is respectfully solicited.

Discussion of objections

The drawings were objected to under 37 CFR 1.84(p)(5) because the reference sign 106' is mentioned in the specification, but not shown in the drawings.

In response thereto, applicants have amended Fig. 1 to show reference number 106. Examiner's approval for the proposed drawing (Fig. 1) change is requested.

The specification was objected to because of informalities. In response thereto, proper correction has been made to the specification by deleting the sub-heading "Summary of the invention" on page 2, line 21.

The Office Action objected to the title of the invention as no being descriptive. Although Applicant respectfully disagrees with this objection, Applicant has amended the title into "FLASH MEMORY STRUCTURE WITH HIGH DIELECTRIC CONSTANT LAYER" in order to comply with the Office Action's objection.

Reconsideration and withdrawal of these objections are respectfully requested.

Discussion for 35 USC 103 rejections

Claims 1, 2 and 4-13 stand rejected under 35 U.S.C.§ 103(a) as being unpatentable over Park (US Patent 6,100,559) in view of Bui (US Patent 6,163,049).

Applicant respectfully traverses these rejections.

Claims 1 and 7 read as follows:

1. A flash memory structure, comprising:
a tunneling oxide layer located upon a substrate;
a floating gate located upon the tunneling oxide layer;
a first oxide layer located upon the floating gate;
a high dielectric constant dielectric layer located upon the first oxide layer, wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8;
a second oxide layer, located upon the high dielectric constant dielectric layer, wherein, together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;
a control gate formed on the second oxide layer of the dielectric stacked layer; and
a source/drain region located in the substrate on the two sides of the floating gate.

7. A flash memory structure, comprising:
a tunneling oxide layer located upon a substrate;
a floating gate located upon the tunneling oxide layer;
a first oxide layer located upon the floating gate;
a high dielectric constant dielectric layer having a dielectric constant greater than 8 located upon the first oxide layer, wherein, together with the oxide layer, a dielectric stacked layer is formed;
a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and
a source/drain region located within the substrate on the two sides of the floating gate.
(Emphasis added)

Applicants submit that claims 1 and 7 patently define over Park and Bui for at least the reason that both Park and Bui fail to disclose at least the features emphasized above.

Park discloses a memory cell 8, including a doped substrate 12, a source/drain 13a, 13b, a tunnel oxide layer 15 and an interpoly dielectric 24 separating a floating gate 16 from a control gate 26. It is noted that the interpoly dielectric 24 typically includes a plurality of films, such as, a bottom film of silicon dioxide, a middle film of silicon nitride and a top film of silicon dioxide. This type of interpoly dielectric layer is commonly referred to as an oxide-nitride-oxide (ONO) layer. Col. 2, lines 20-24. In other words, Part teaches a flash memory with a conventional ONO layer placed in between a floating gate and a control gate.

While the present invention is intended to reduce the voltage value required in a flash memory by replacing the conventional ONO layer with a first oxide layer and a second oxide layer having a high dielectric constant dielectric layer in between (claim 1), or with an oxide layer and a high dielectric constant dielectric layer (claim 7). Park not only fails to teach the high dielectric

constant dielectric layer, but, more importantly, also fails to teach or suggest how the high dielectric constant dielectric layer is combined into a flash memory structure to achieve the intended goal of reducing voltage value

The Office Action cited Bui to teach a dielectric layer having a dielectric constant greater than 8, such as aluminum oxide, and asserted that it would have been obvious to one skilled in the art to modify the device of Park to include an aluminum oxide as disclosed in Bui.

Applicant respectfully disagrees. It is believed that the proposed combination is improper for the reasons set forth below.

Bui teaches a flash memory having a floating gate and a control gate separated by a distance corresponding to at least a minimum design data retention. This distance is managed by depositing a first oxide dielectric layer on the floating gate at a first thickness, a nitride dielectric layer on the first oxide dielectric layer at a second thickness, and a second oxide dielectric layer on the nitride dielectric layer at a third thickness. What different from Park is that the first oxide layer and/or the second oxide layer has a high dielectric constant, e.g. greater than 10. Col. 2, lines 25-30. But the stack between the floating gate and the control gate in Bui still is a composite ONO layer. Col. 3, lines 46-48. In other words, the high dielectric constant dielectric layer(s) in Bui is not used to replace the nitride dielectric layer.

To combine the references, there must be some suggestion to do so. *See In re Chu*, 66 F.3d 292, 36 USPQ2d 1089 (Fed. Cir. 1995) ("Although a prior art device could have been turned upside down, that did not make the modification obvious unless the prior art fairly suggested the desirability of turning the device upside down." citing *In re Gordon*, 733 F.2d 900, 902, 221 USPQ2d 1125, 1227 (Fed. Cir. 1984)). Such requisite suggestion for the proposed combination of Park and Bui is not shown to have been provided either by Park and Bui, or by common knowledge of a person skilled in the art. Applicant has never claimed that a high dielectric constant (such as higher than 8) dielectric layer is new, but it is used in a novel way in the present invention to achieve an intended purpose. The fact that Bui uses a composite ONO layer with high dielectric constant dielectric layer(s) together with a nitride layer indicates that Bui does not suggest the proposed combination.

Furthermore, It is improper to combine references where to modify the primary reference

would "destroy its structural identity and mode of operation." *Ex parte Jackson,* 146 USPQ 409, 410 (PTO Bd. App. 1964). As discussed in the specification, the silicon nitride layer of an ONO layer in a flash memory structure has its unique functions. Page 3, paragraphs [0007] and [0008]. If Park were modified as proposed by replacing the silicon nitride layer in ONO layer 24 with a high dielectric constant dielectric layer of Bui, the ONO layer structure would be destroyed, the structural identity and mode of operation of Park's device would be destroyed.

Therefore, the proposed combination of Park and Bui is improper and cannot used to support the rejections under 35 USC 103.

For at least the reasons discussed above, Applicant respectfully submits that claims 1 and 7 patently defines over the cited references. For at least the same reasons, all depending claims 2, 4-6, and 8-12 patently define over the cited references and should be allowed. Accordingly, the rejection under §103 should be withdrawn.

Claim 13 recites an Al_2O_3 layer located in between, and in direct contact with, a floating gate and a control gate. This feature is not taught by either Park or Bui. Therefore, claim 13 is patentable over Park and Bui.

CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGE

IN THE SPECIFICATION

On page 1, the title of invention has been amended as follows:

FLASH MEMORY STRUCTURE WITH HIGH DIELECTRIC CONSTANT LAYER

On page 2, line 21, the subheading [SUMMARY OF THE INVENTION] has been deleted.

Fig. 1 has been amended.